

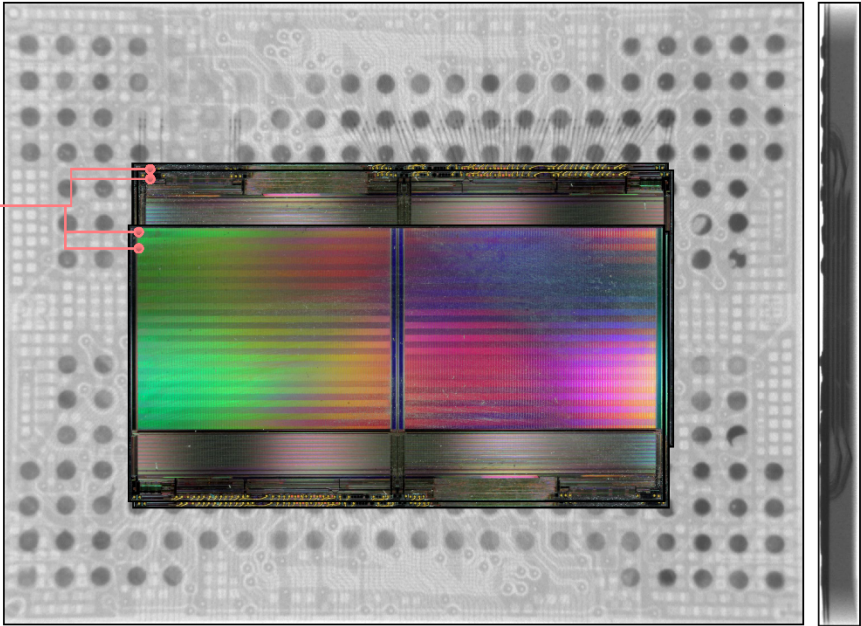
# EXHIBIT C

**U.S. Patent No. 6,724,241 (“’241 Patent”)**

Dell/EMC products with SanDisk/Toshiba 64L 3D NAND flash chips, including without limitation the Dell/EMC XPS 15 2-in-1 9575 (“Accused Products”), infringe at least Claims 1-3, 6-8, and 11 of the ’241 Patent. While the infringing structure and functionality of the Accused Products is illustrated below using the Dell/EMC XPS 15 2-in-1 9575 as an example, all Accused Products operate in substantially the same way for purposes of infringement.

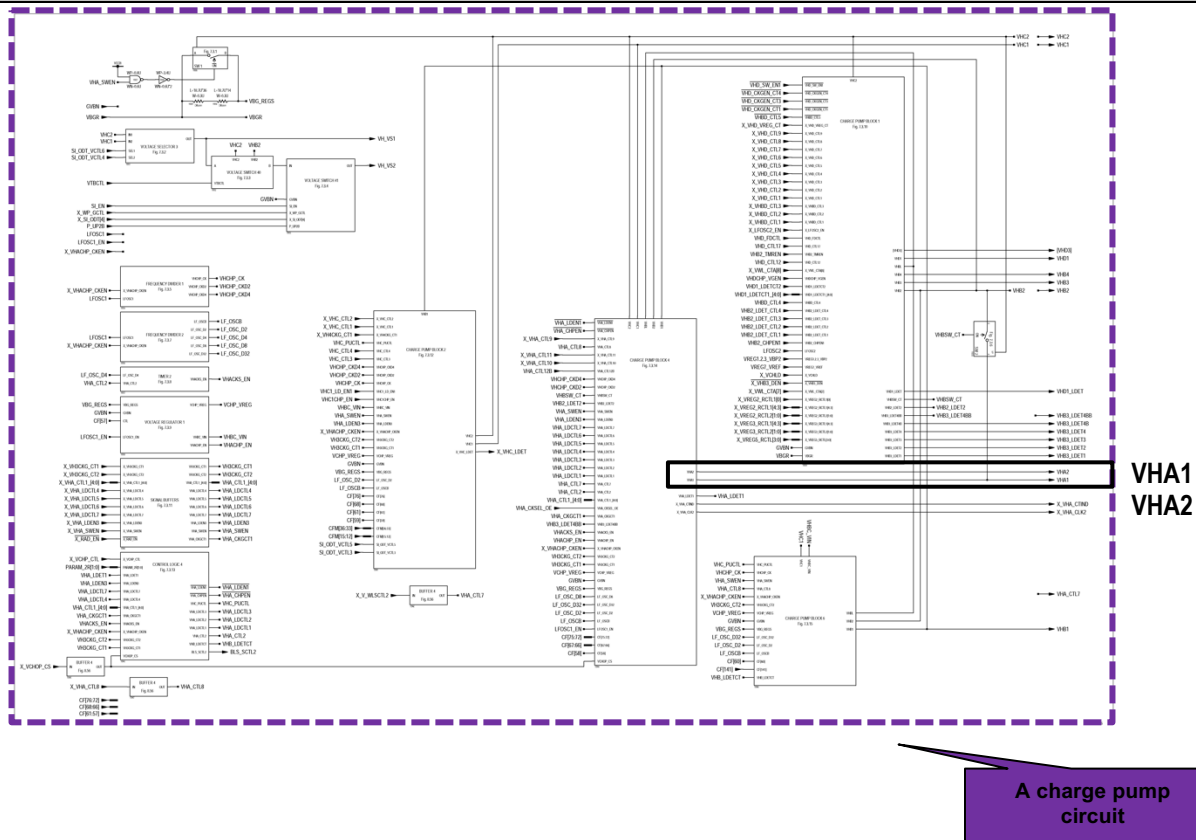
**Claim 1**

Claim 1	Accused Products
1[pre]. A charge pump circuit for generating a charge pump voltage having minimal voltage ripples, comprising:	<p>To the extent the preamble is limiting, each Accused Product includes a charge pump circuit for generating a charge pump voltage having minimal voltage ripples.</p> <p>For example, the Dell/EMC XPS 15 2-in-1 9575 includes the charge pump circuit of the SanDisk/Toshiba 3D NAND flash chip, die identifier FRN1256G.</p> <p><i>See, e.g.:</i></p>

Claim 1	Accused Products
	<div data-bbox="688 267 1087 341"><p>76 - Toshiba #TH58TFT0T23BADE Multichip Memory - 128 GB 3D TLC NAND Flash (4-Die Pkg.) Pkg Size: 18.02 x 14.01 mm</p></div> <div data-bbox="688 511 936 584"><p>76.1 - Toshiba #FRN1256G 3D TLC NAND Flash Memory - 32 GB Die Size: 12.15 x 6.28 mm</p></div> <div data-bbox="688 885 844 925"><p>Function: Memory: Non-Volatile</p></div> <div data-bbox="940 344 1795 966"></div> <p data-bbox="634 987 1810 1023">Source: TechInsights Deep Dive Teardown, Dell/EMC XPS 15 2-in-1 9575 ID306753-GDd</p>

## Claim 1

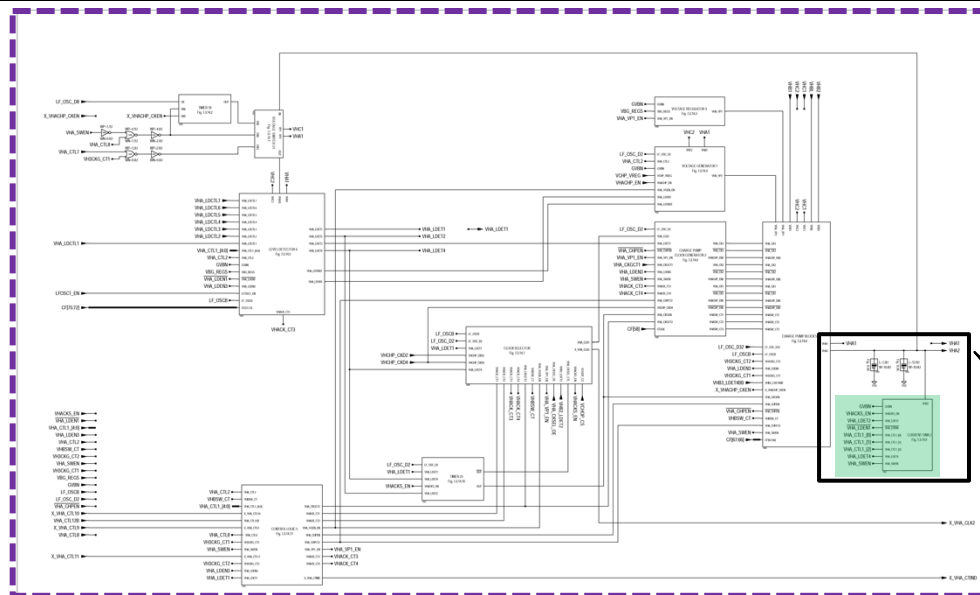
## Accused Products



Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138\_064G 3D NAND Flash, Figure 7.3 Charge Pump System

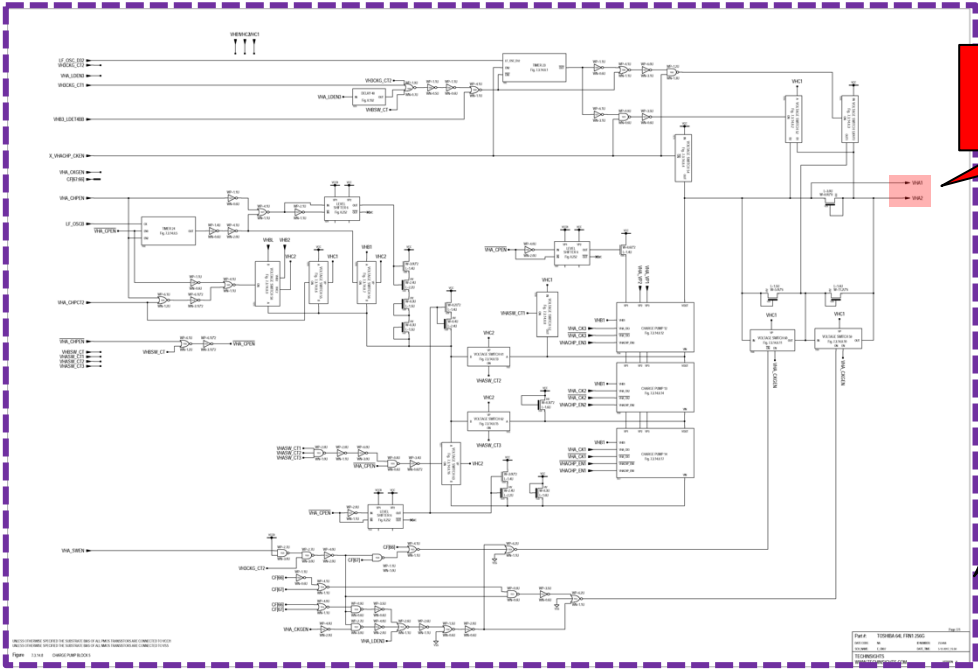
## Claim 1

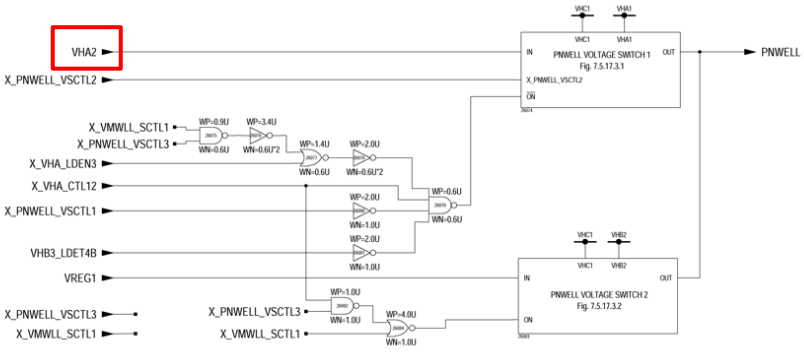
## Accused Products

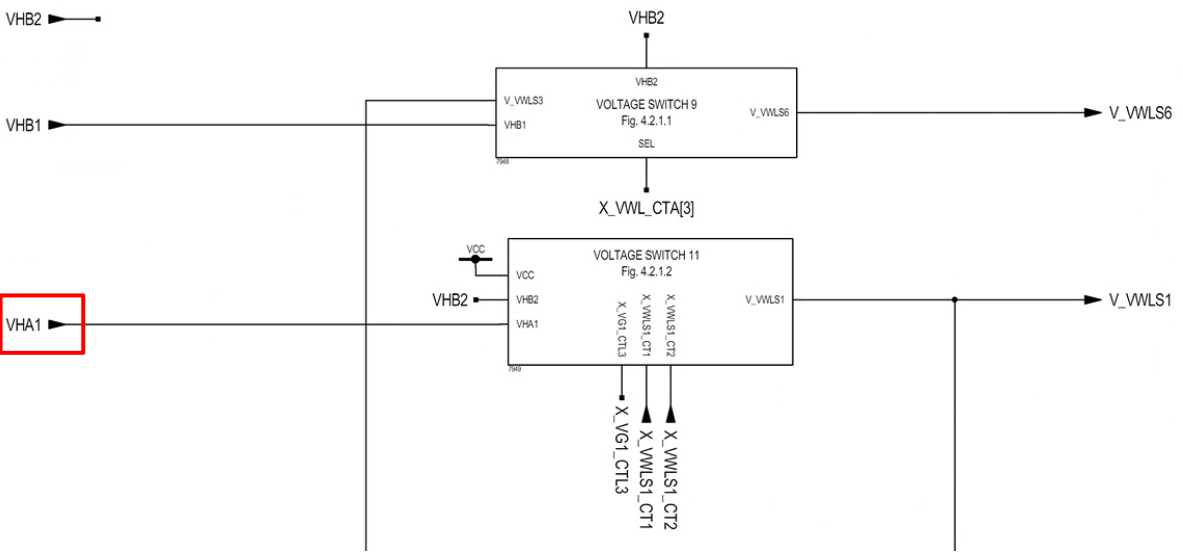


having  
minimal  
voltage  
ripples

Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138\_064G 3D NAND Flash, Figure 7.3 Charge Pump System

Claim 1	Accused Products
	<div data-bbox="640 264 1612 930"></div> <div data-bbox="1591 305 1871 412" style="background-color: red; color: black; padding: 5px;"><p>for generating a charge pump voltage (VHA1, VHA2)</p></div> <div data-bbox="1623 483 1843 574" style="background-color: white; color: black; padding: 5px;"><p>VHA1 and VHA2 are driven by the same pumping circuit</p></div> <div data-bbox="1629 646 1839 716" style="background-color: purple; color: white; padding: 5px;"><p>A charge pump circuit</p></div> <p data-bbox="632 992 1829 1062">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

Claim 1	Accused Products
	<p data-bbox="688 272 1255 332"><b>Charge pump output voltage VHA2 is provided to high voltage switches to selectively drive PNWELL.</b></p>  <p data-bbox="634 776 1831 844">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.5.17.3 PNWELL Voltage Selector</p>

Claim 1	Accused Products
	<p><b>Charge pump output voltage VHA1 is provided to high voltage switches to selectively drive wordline circuits.</b></p>  <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
<p>1[a] a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages;</p>	<p>Each Accused Product includes a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages.</p> <p>For example, in the pumping circuit of the Dell/EMC XPS 15 2-in-1 9575, 1, 2, or 3 main stages can be enabled for operation. Supply voltage can be selected from external VCC or internally generated pumped voltages VHBL or VHB1. VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72) adjusts the</p>



Claim 1	Accused Products
	<p>output reference voltage by shorting out resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping. VHA_CK2 and VHA_CK2* drive the middle stage of the pumping circuit. VHA_PH2 non-overlapping clocks drive Charge Pump 13. When VHA_PH2 clocks are suspended the pump stops operating so that VHA1 is limited to the voltage set by the level detector.</p> <p><i>See, e.g.:</i></p>

# Claim 1

## Accused Products

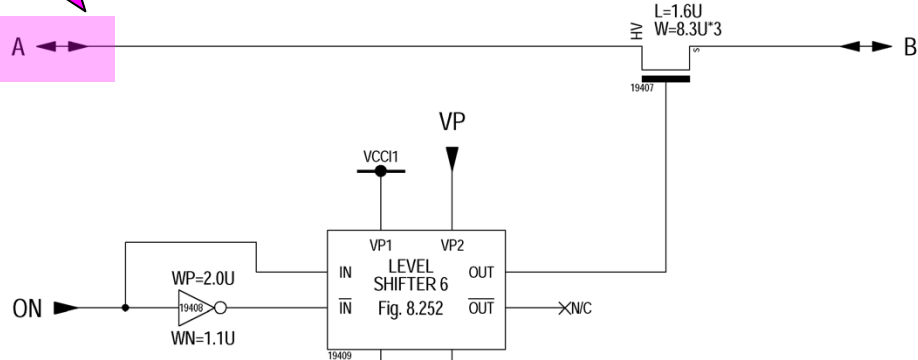
operable to receive a supply voltage

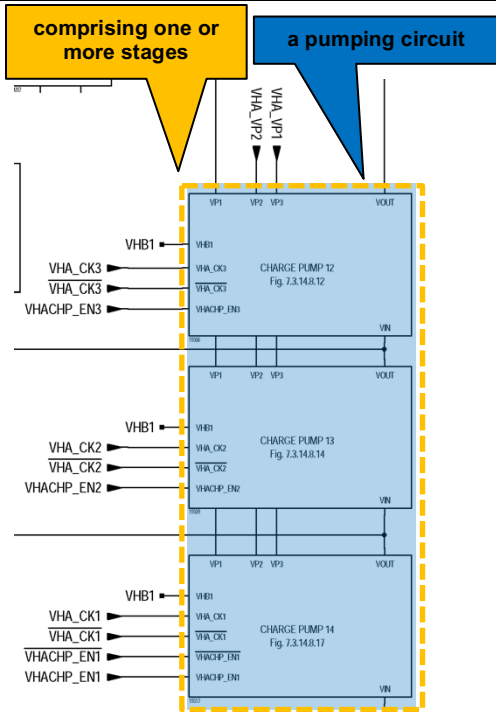
a pumping circuit

CHARGE PUMP BLOCK 5

FIG. 7.3.14.8

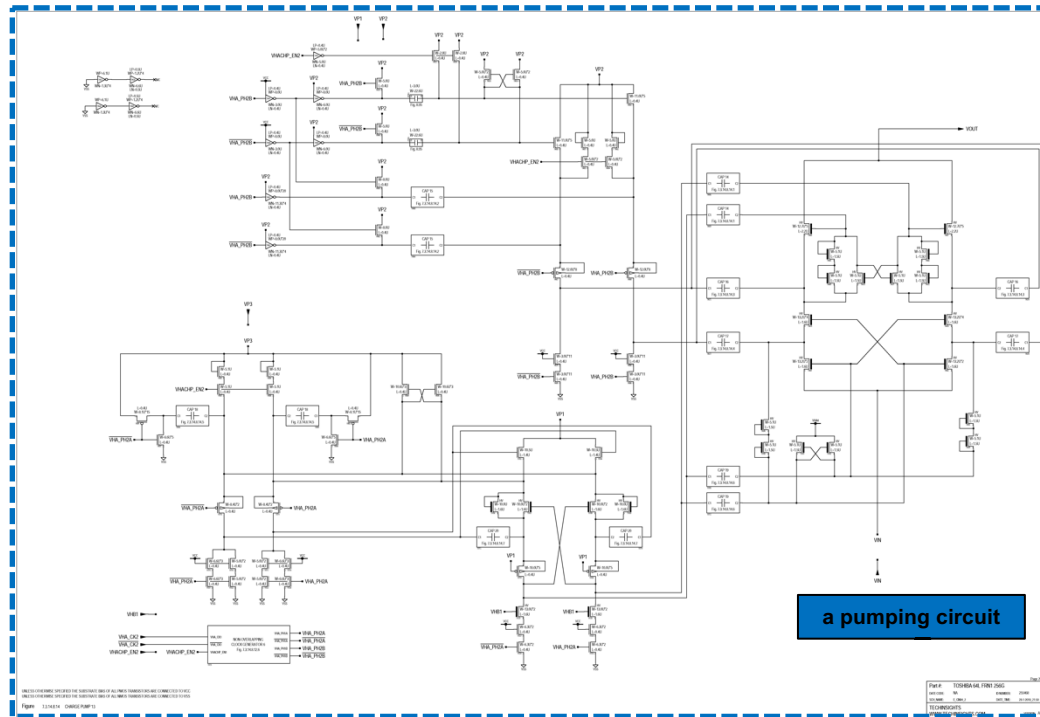
Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138\_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5

Claim 1	Accused Products
	<p data-bbox="632 264 963 329"><b>operable to receive a supply voltage (VCC)</b></p>  <p data-bbox="632 808 1829 881">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.6 Voltage Switch 55</p>

Claim 1	Accused Products
	 <p>The diagram illustrates a multi-stage charge pump circuit, labeled 'comprising one or more stages' and 'a pumping circuit'. It consists of three identical charge pump blocks stacked vertically, each labeled 'CHARGE PUMP 12', 'CHARGE PUMP 13', and 'CHARGE PUMP 14' respectively. Each block has four inputs on the left: VHB1, VHA_CK3, VHA_CK3, and VHACHP_EN3 for Pump 12; VHB1, VHA_CK2, VHA_CK2, and VHACHP_EN2 for Pump 13; and VHB1, VHA_CK1, VHA_CK1, and VHACHP_EN1 for Pump 14. Each block has four outputs on the right: VP1, VP2, VP3, and VOUT. The outputs of the first two pumps (VP1, VP2, VP3) are connected to the inputs of the third pump. The final output VOUT is connected to the output of the third pump. The diagram is enclosed in a dashed yellow box.</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

## Claim 1

## Accused Products



Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138\_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13

<p>Claim 1</p>	<p>Accused Products</p>
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

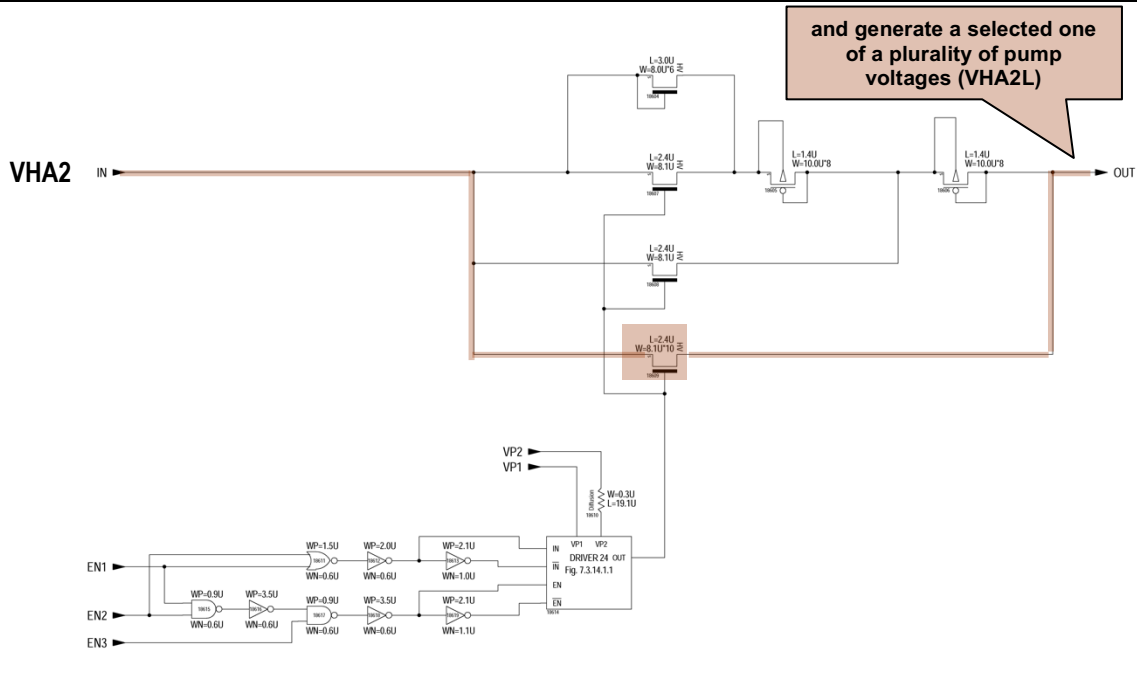
# Claim 1

## Accused Products

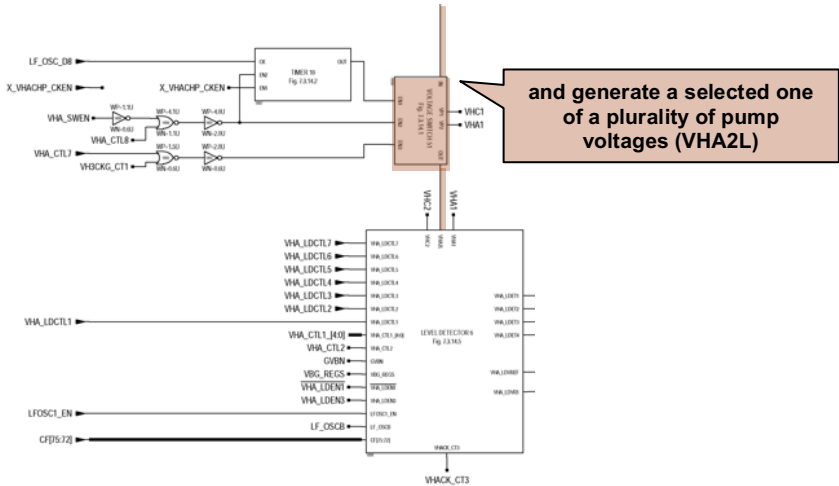
and generate a selected one of a plurality of pump voltages (VHA1, VHA2)

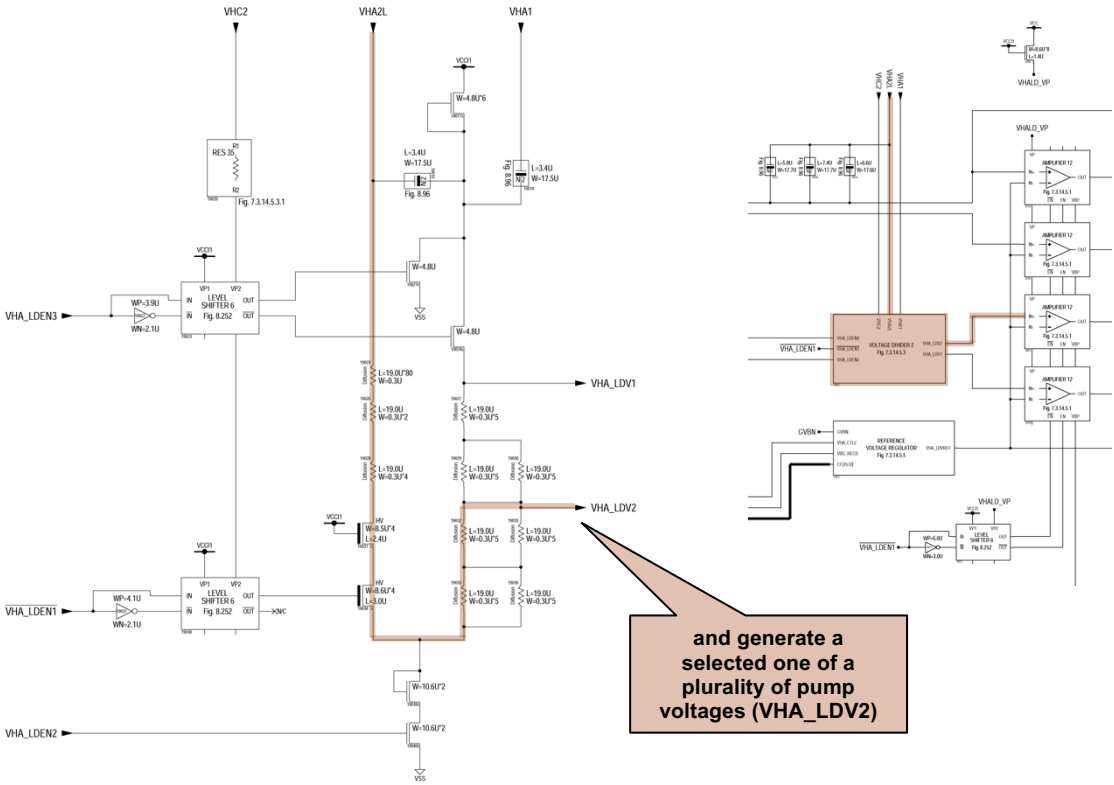
FIG. 13-14 CHARGE PUMP BLOCK 4

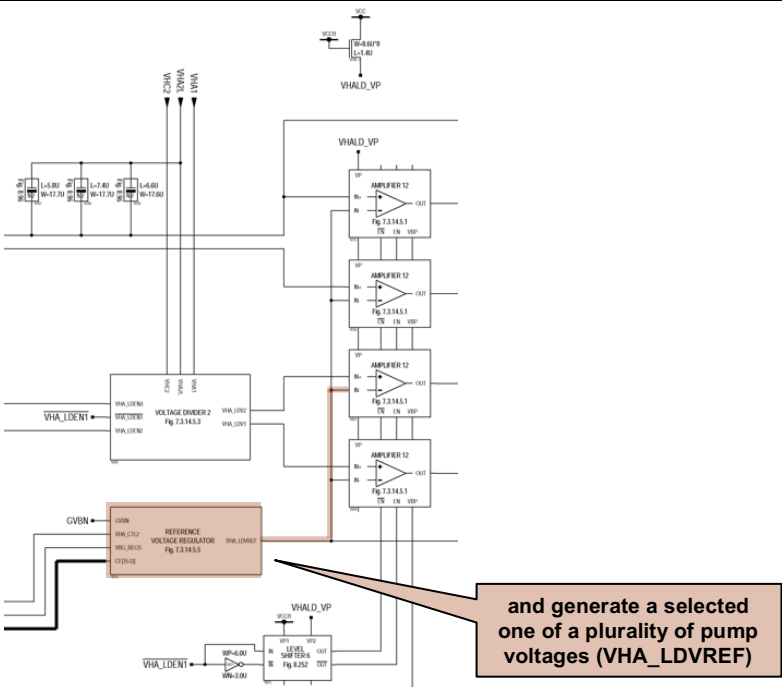
Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138\_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4

Claim 1	Accused Products
	 <p>and generate a selected one of a plurality of pump voltages (VHA2L)</p> <p>VHA2 IN</p> <p>OUT</p> <p>VP2</p> <p>VP1</p> <p>EN1</p> <p>EN2</p> <p>EN3</p> <p>WP-1.5U</p> <p>WN-0.6U</p> <p>WP-2.0U</p> <p>WN-0.6U</p> <p>WP-2.1U</p> <p>WN-1.0U</p> <p>WP-0.9U</p> <p>WN-0.6U</p> <p>WP-3.5U</p> <p>WN-0.6U</p> <p>WP-0.9U</p> <p>WN-0.6U</p> <p>WP-3.5U</p> <p>WN-0.6U</p> <p>WP-2.1U</p> <p>WN-1.1U</p> <p>W-0.3U</p> <p>L-19.1U</p> <p>DRIVER 24</p> <p>Fig. 7.3.14.1.1</p>
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.1 Voltage Switch 51</p>



Claim 1	Accused Products
	 <p>and generate a selected one of a plurality of pump voltages (VHA2L)</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

Claim 1	Accused Products
	 <p>and generate a selected one of a plurality of pump voltages (VHA_LDV2)</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2; Figure 7.3.14.5 Level Detector 6</p>

Claim 1	Accused Products
	 <p>and generate a selected one of a plurality of pump voltages (VHA_LDVPREF)</p>
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>

### Claim 1

### Accused Products

The circuit diagram illustrates a reference voltage regulator. It features several PMOS and NMOS transistors, resistors, and capacitors. Key components include:

- VDD**: Power supply connection.
- VSS**: Ground connection.
- CVBIN**: Input capacitor.
- VHA\_CTL2**: Control signal input.
- VHC\_REGS**: Register output signal.
- VHA\_LDREF**: Output reference voltage.

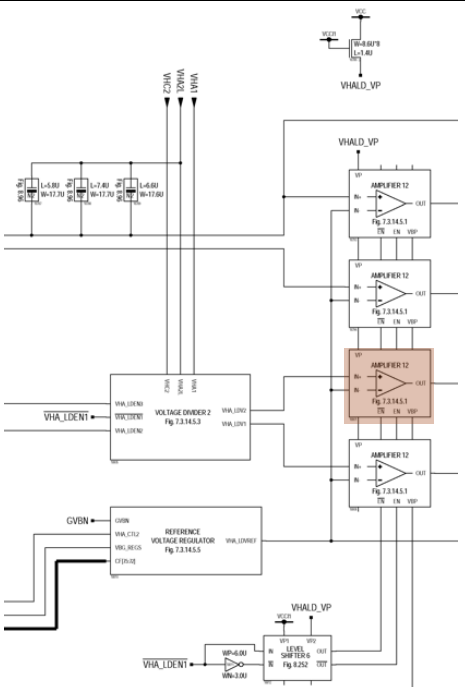
A callout box highlights the output stage, stating: "and generate a selected one of a plurality of pump voltages (VHA\_LDREF)".

**Figure 7.3.14.5.5 REFERENCE VOLTAGE REGULATOR**

UNLESS OTHERWISE SPECIFIED THE SUBSTRATE BIAS OF ALL PMOS TRANSISTORS ARE CONNECTED TO VDD  
UNLESS OTHERWISE SPECIFIED THE SUBSTRATE BIAS OF ALL NMOS TRANSISTORS ARE CONNECTED TO VSS

Part #: TOSHIBA 64L FRM 256G  
SHEET CODE: W- C-0000 DATE TIME: 19.10.2011.18:00  
TECHINSIGHTS  
WWW.TECHINSIGHTS.COM

Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138\_064G 3D NAND Flash, Figure 7.3.14.5.5 Reference Voltage Regulator

Claim 1	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>

### Claim 1

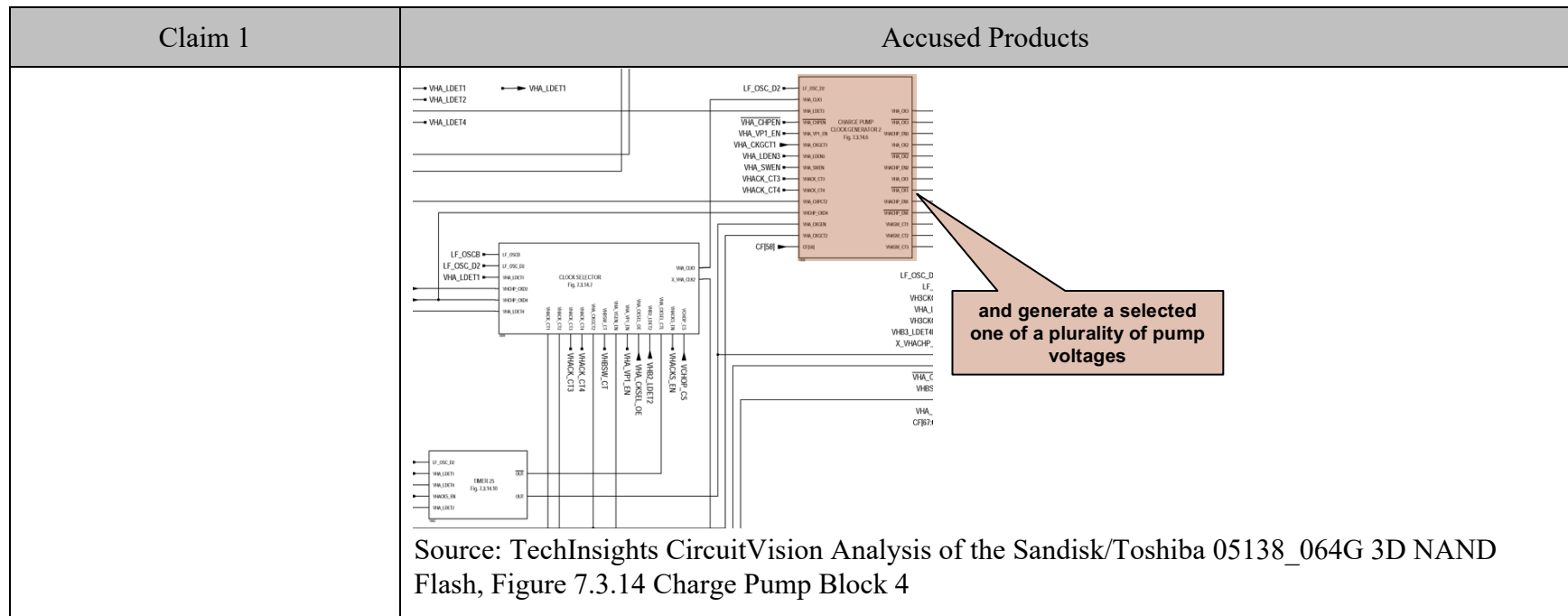
### Accused Products

and generate a selected one of a plurality of pump voltages

VH\_ADET3 = 0

Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138\_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6

Claim 1	Accused Products
	<p>VHA_LDET3 = 1 Disables VHA_CK2 pump clock to 1 level</p> <p>VHA_CK2 = 1 VHA_CK2* = 0</p> <p>and generate a selected one of a plurality of pump voltages</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.6 Charge Pump Clock Generator 2</p>





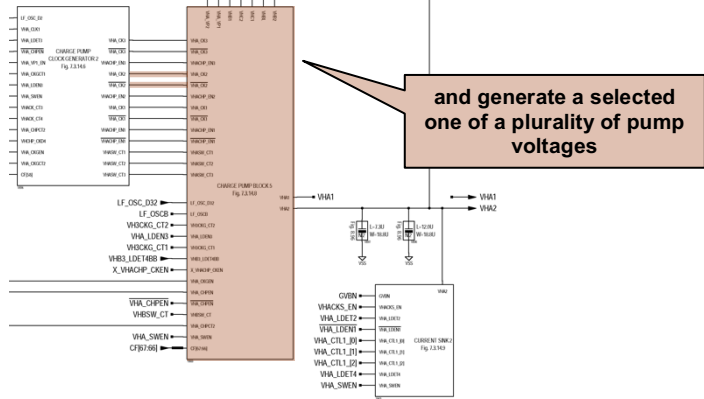
# Claim 1

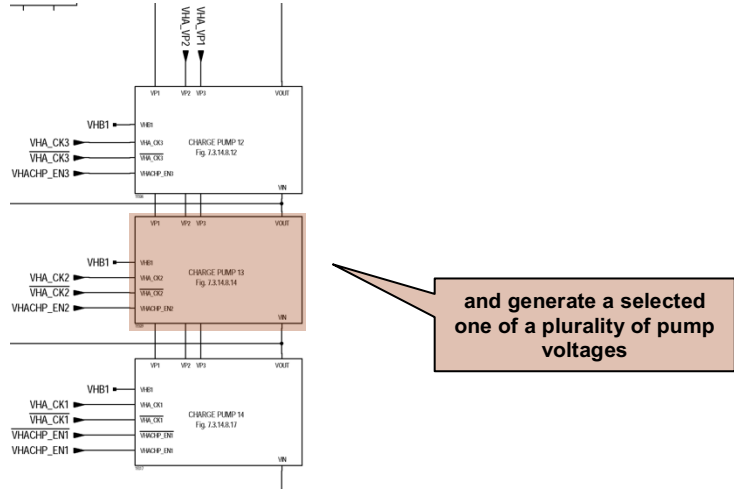
## Accused Products

and generate a selected one of a plurality of pump voltages

a pumping circuit

Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138\_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5

Claim 1	Accused Products
	 <p>and generate a selected one of a plurality of pump voltages</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

Claim 1	Accused Products
	 <p>The diagram shows three charge pump blocks stacked vertically. Each block has multiple input and output pins. The top block is labeled 'CHARGE PUMP 12 Fig. 7.3.14.8.12'. The middle block is labeled 'CHARGE PUMP 13 Fig. 7.3.14.8.13' and is highlighted with a brown background. The bottom block is labeled 'CHARGE PUMP 14 Fig. 7.3.14.8.14'. A callout box with a pointer to the middle block contains the text: 'and generate a selected one of a plurality of pump voltages'.</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

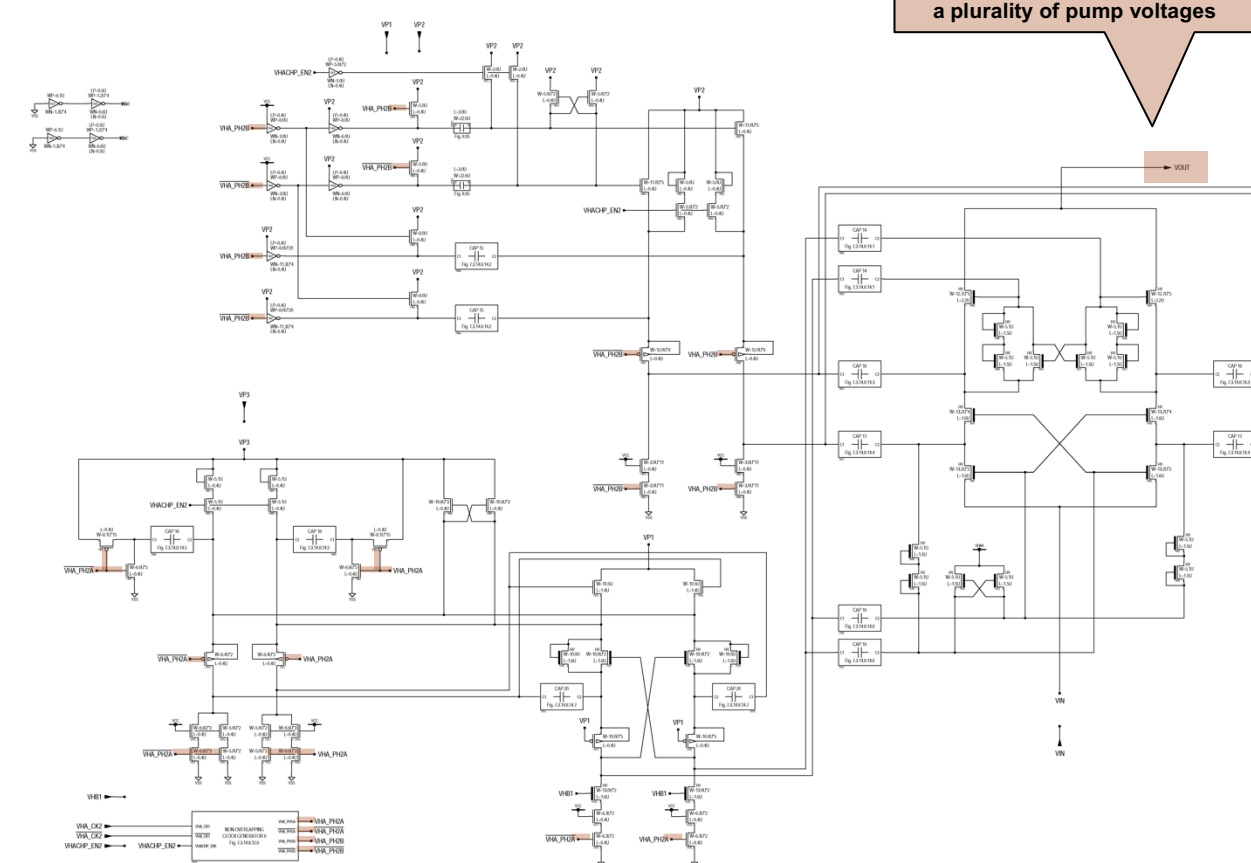
### Claim 1

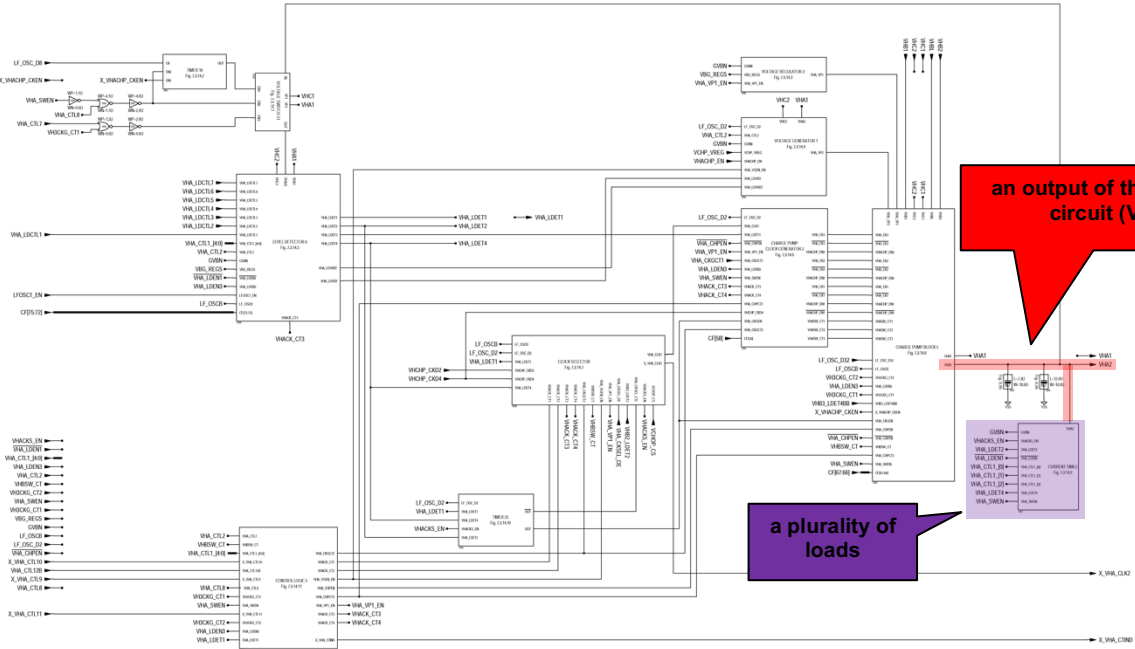
Accused Products

and generate a selected one of a plurality of pump voltages

Claim 1	Accused Products
<p>VHA_CK2 VHA_CK2*</p>	<div data-bbox="636 308 1757 941"> <p>VHA_PH2A VHA_PH2A* VHA_PH2B VHA_PH2B*</p> </div> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.12.6 Non-Overlapping Clock Generator 6</p>

[illegible]

<p>Claim 1</p>	<p>Accused Products</p>
<p>1[b] a plurality of loads selectively coupleable to an output of the pumping circuit,</p>	<div data-bbox="1516 263 1879 428" style="border: 1px solid black; padding: 5px; margin-bottom: 10px;"> <p>and generate a selected one of a plurality of pump voltages</p> </div>  <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>
	<p>Each Accused Product includes a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage.</p>

Claim 1	Accused Products
<p>each load associated with a specific pump voltage; and</p>	<p>For example, in the Dell/EMC XPS 15 2-in-1 9575, VHA2 is an output of the pumping circuit. A plurality of loads (contained within Current Sink 2) can be selectively coupled to an output of the pumping circuit (for example VHA2). VHA2 is connected to pumping circuit output VHA1 through Voltage Switches 59 and 60. VHA1 is connected to wordline decoders during read or program operations. Read, program and erase operations require different voltages. Each load is associated with a specific pump voltage to carry out these functions.</p> <p><i>See, e.g.:</i></p>  <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

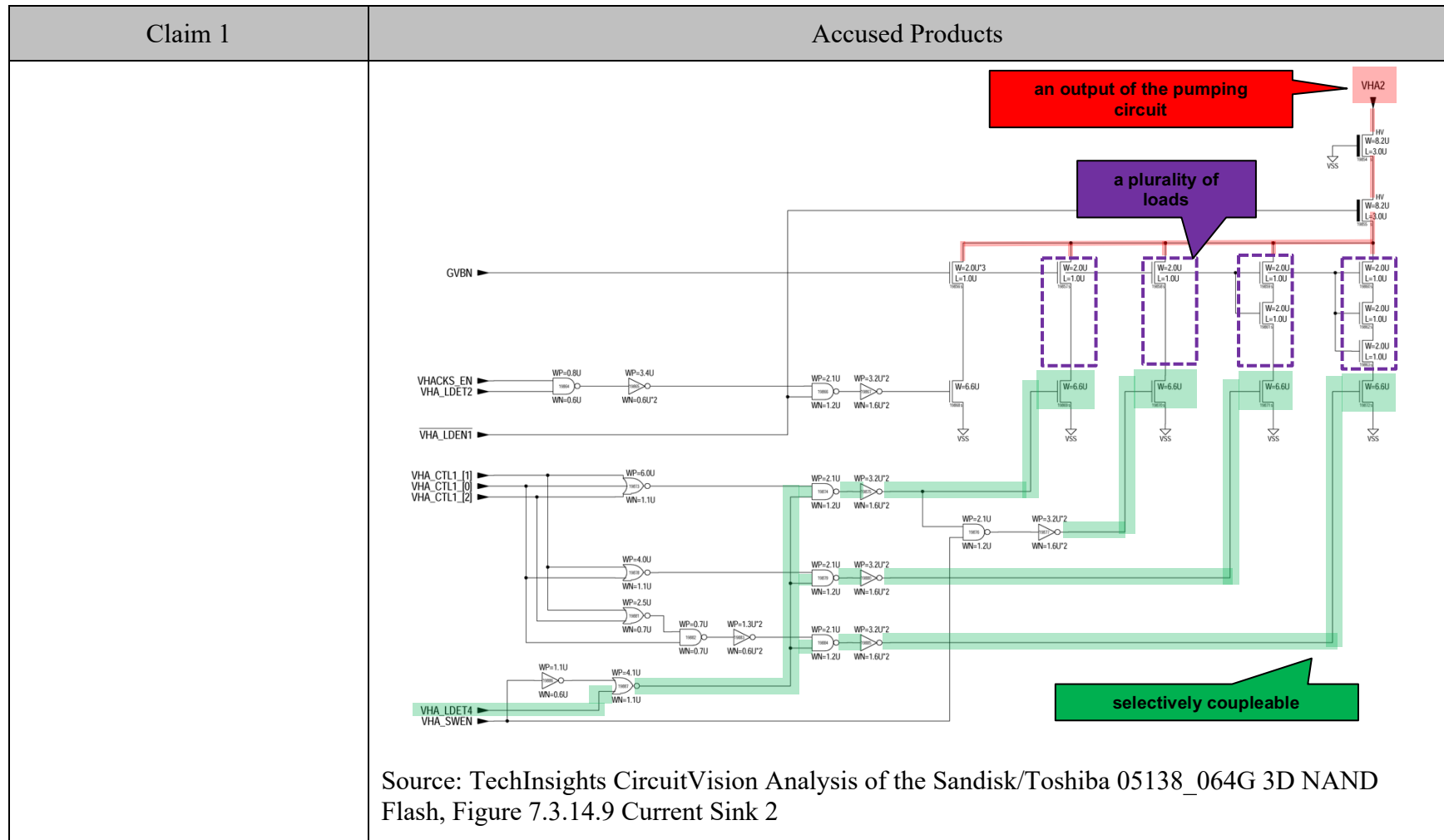


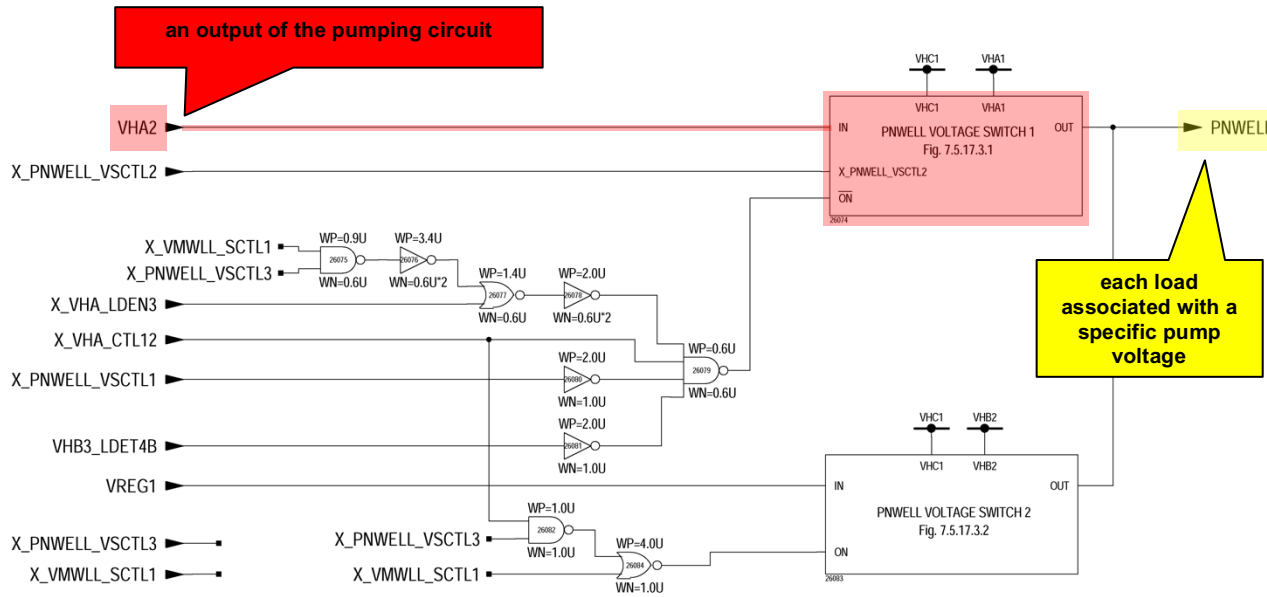
Claim 1

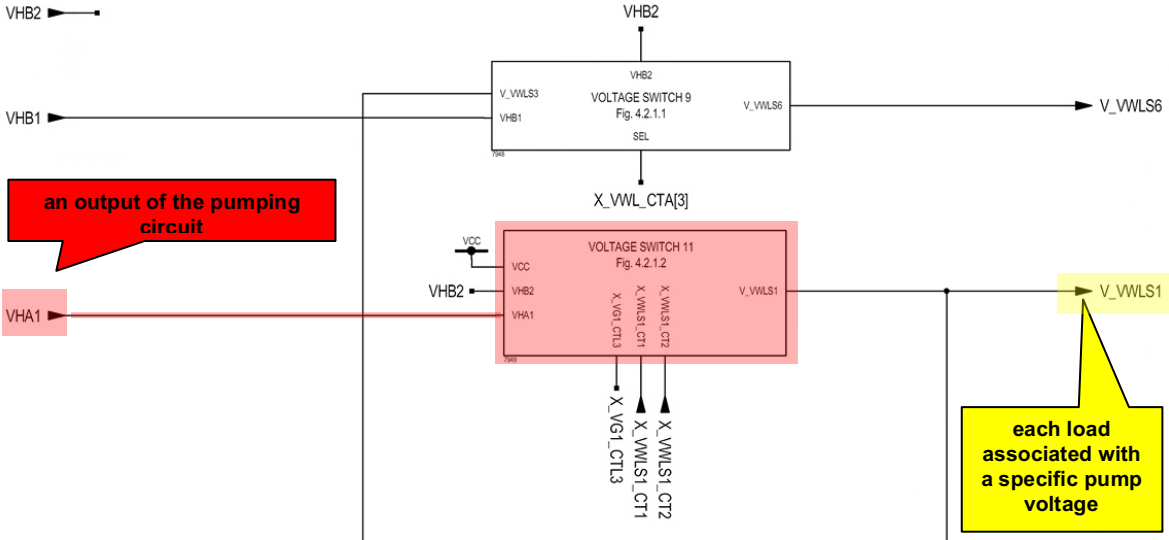
Accused Products

The diagram illustrates a complex charge pump circuit, identified as 'Charge Pump Block 5'. It features a central core of transistors (MOSFETs) and capacitors, with various control signals at the inputs and outputs. Key input signals include VDD, VSS, VDDP, VSSP, VDDN, VSSN, VDDP1, VSSP1, VDDP2, VSSP2, VDDP3, VSSP3, VDDP4, VSSP4, VDDP5, VSSP5, VDDP6, VSSP6, VDDP7, VSSP7, VDDP8, VSSP8, VDDP9, VSSP9, VDDP10, VSSP10, VDDP11, VSSP11, VDDP12, VSSP12, VDDP13, VSSP13, VDDP14, VSSP14, VDDP15, VSSP15, VDDP16, VSSP16, VDDP17, VSSP17, VDDP18, VSSP18, VDDP19, VSSP19, VDDP20, VSSP20, VDDP21, VSSP21, VDDP22, VSSP22, VDDP23, VSSP23, VDDP24, VSSP24, VDDP25, VSSP25, VDDP26, VSSP26, VDDP27, VSSP27, VDDP28, VSSP28, VDDP29, VSSP29, VDDP30, VSSP30, VDDP31, VSSP31, VDDP32, VSSP32, VDDP33, VSSP33, VDDP34, VSSP34, VDDP35, VSSP35, VDDP36, VSSP36, VDDP37, VSSP37, VDDP38, VSSP38, VDDP39, VSSP39, VDDP40, VSSP40, VDDP41, VSSP41, VDDP42, VSSP42, VDDP43, VSSP43, VDDP44, VSSP44, VDDP45, VSSP45, VDDP46, VSSP46, VDDP47, VSSP47, VDDP48, VSSP48, VDDP49, VSSP49, VDDP50, VSSP50, VDDP51, VSSP51, VDDP52, VSSP52, VDDP53, VSSP53, VDDP54, VSSP54, VDDP55, VSSP55, VDDP56, VSSP56, VDDP57, VSSP57, VDDP58, VSSP58, VDDP59, VSSP59, VDDP60, VSSP60, VDDP61, VSSP61, VDDP62, VSSP62, VDDP63, VSSP63, VDDP64, VSSP64, VDDP65, VSSP65, VDDP66, VSSP66, VDDP67, VSSP67, VDDP68, VSSP68, VDDP69, VSSP69, VDDP70, VSSP70, VDDP71, VSSP71, VDDP72, VSSP72, VDDP73, VSSP73, VDDP74, VSSP74, VDDP75, VSSP75, VDDP76, VSSP76, VDDP77, VSSP77, VDDP78, VSSP78, VDDP79, VSSP79, VDDP80, VSSP80, VDDP81, VSSP81, VDDP82, VSSP82, VDDP83, VSSP83, VDDP84, VSSP84, VDDP85, VSSP85, VDDP86, VSSP86, VDDP87, VSSP87, VDDP88, VSSP88, VDDP89, VSSP89, VDDP90, VSSP90, VDDP91, VSSP91, VDDP92, VSSP92, VDDP93, VSSP93, VDDP94, VSSP94, VDDP95, VSSP95, VDDP96, VSSP96, VDDP97, VSSP97, VDDP98, VSSP98, VDDP99, VSSP99, VDDP100, VSSP100. The circuit includes several capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100) and various control signals (VDD, VSS, VDDP, VSSP, VDDN, VSSN, VDDP1, VSSP1, VDDP2, VSSP2, VDDP3, VSSP3, VDDP4, VSSP4, VDDP5, VSSP5, VDDP6, VSSP6, VDDP7, VSSP7, VDDP8, VSSP8, VDDP9, VSSP9, VDDP10, VSSP10, VDDP11, VSSP11, VDDP12, VSSP12, VDDP13, VSSP13, VDDP14, VSSP14, VDDP15, VSSP15, VDDP16, VSSP16, VDDP17, VSSP17, VDDP18, VSSP18, VDDP19, VSSP19, VDDP20, VSSP20, VDDP21, VSSP21, VDDP22, VSSP22, VDDP23, VSSP23, VDDP24, VSSP24, VDDP25, VSSP25, VDDP26, VSSP26, VDDP27, VSSP27, VDDP28, VSSP28, VDDP29, VSSP29, VDDP30, VSSP30, VDDP31, VSSP31, VDDP32, VSSP32, VDDP33, VSSP33, VDDP34, VSSP34, VDDP35, VSSP35, VDDP36, VSSP36, VDDP37, VSSP37, VDDP38, VSSP38, VDDP39, VSSP39, VDDP40, VSSP40, VDDP41, VSSP41, VDDP42, VSSP42, VDDP43, VSSP43, VDDP44, VSSP44, VDDP45, VSSP45, VDDP46, VSSP46, VDDP47, VSSP47, VDDP48, VSSP48, VDDP49, VSSP49, VDDP50, VSSP50, VDDP51, VSSP51, VDDP52, VSSP52, VDDP53, VSSP53, VDDP54, VSSP54, VDDP55, VSSP55, VDDP56, VSSP56, VDDP57, VSSP57, VDDP58, VSSP58, VDDP59, VSSP59, VDDP60, VSSP60, VDDP61, VSSP61, VDDP62, VSSP62, VDDP63, VSSP63, VDDP64, VSSP64, VDDP65, VSSP65, VDDP66, VSSP66, VDDP67, VSSP67, VDDP68, VSSP68, VDDP69, VSSP69, VDDP70, VSSP70, VDDP71, VSSP71, VDDP72, VSSP72, VDDP73, VSSP73, VDDP74, VSSP74, VDDP75, VSSP75, VDDP76, VSSP76, VDDP77, VSSP77, VDDP78, VSSP78, VDDP79, VSSP79, VDDP80, VSSP80, VDDP81, VSSP81, VDDP82, VSSP82, VDDP83, VSSP83, VDDP84, VSSP84, VDDP85, VSSP85, VDDP86, VSSP86, VDDP87, VSSP87, VDDP88, VSSP88, VDDP89, VSSP89, VDDP90, VSSP90, VDDP91, VSSP91, VDDP92, VSSP92, VDDP93, VSSP93, VDDP94, VSSP94, VDDP95, VSSP95, VDDP96, VSSP96, VDDP97, VSSP97, VDDP98, VSSP98, VDDP99, VSSP99, VDDP100, VSSP100). A red arrow points to a specific output node labeled 'an output of the pumping circuit'.

Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138\_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5



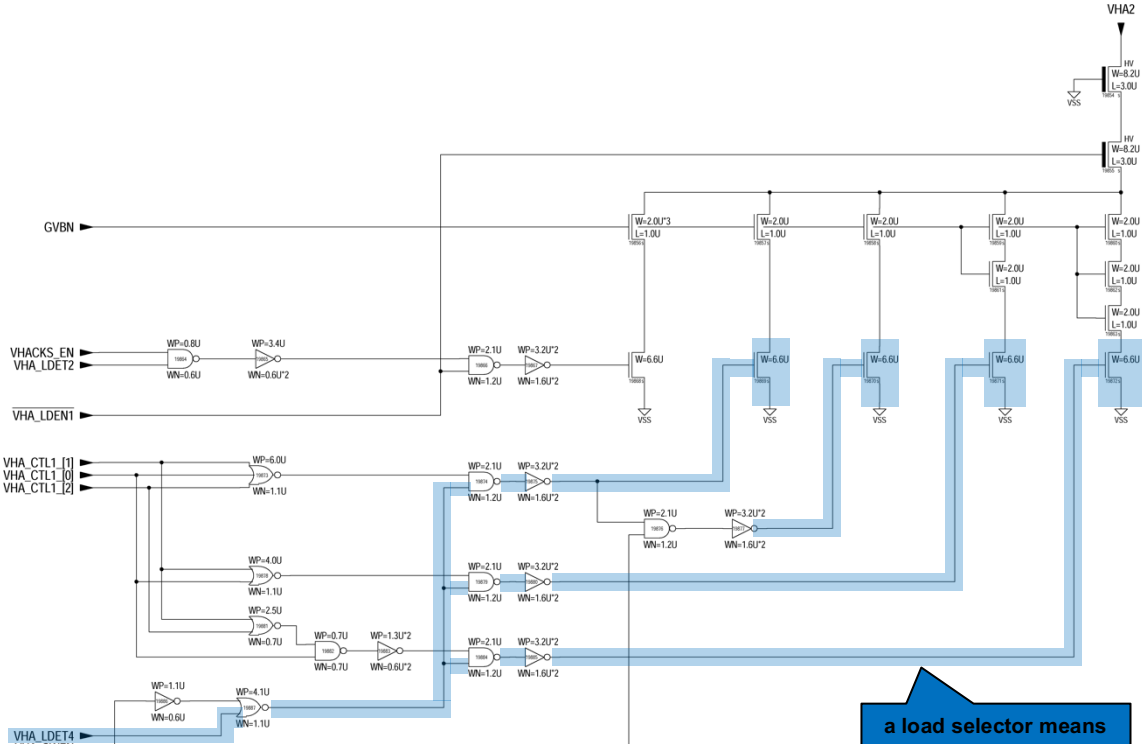
Claim 1	Accused Products
	 <p>an output of the pumping circuit</p> <p>VHA2</p> <p>X_PNWELL_VSCTL2</p> <p>X_VMWLL_SCTL1</p> <p>X_PNWELL_VSCTL3</p> <p>X_VHA_LDEN3</p> <p>X_VHA_CTL12</p> <p>X_PNWELL_VSCTL1</p> <p>VHB3_LDET4B</p> <p>VREG1</p> <p>X_PNWELL_VSCTL3</p> <p>X_VMWLL_SCTL1</p> <p>PNWELL VOLTAGE SWITCH 1 Fig. 7.5.17.3.1</p> <p>PNWELL VOLTAGE SWITCH 2 Fig. 7.5.17.3.2</p> <p>PNWELL</p> <p>each load associated with a specific pump voltage</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.5.17.3 PNWELL Voltage Selector</p>

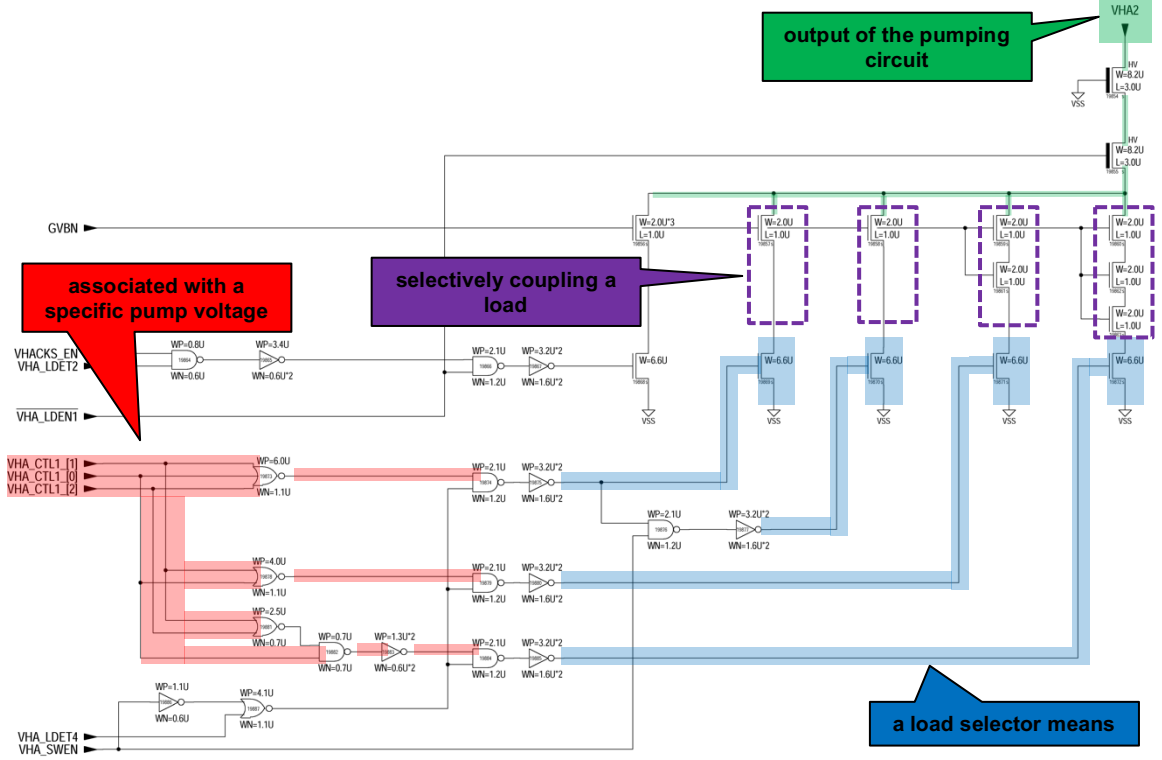
Claim 1	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
<p>1[c] a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit</p>	<p>Each Accused Product includes a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.</p> <p>For example, in the Dell/EMC XPS 15 2-in-1 9575, the highlighted transistors below and their respective gate control signals form a load selector means. The output signal VHA_LDET4 from Level Detector 6 forms part of the load selector means. For example, the gate control signals are generated in part by a charge pump control signal (VHA_CTL1). This 3 bit value selectively couples a load associated with a specific pump voltage.</p> <p><i>See, e.g.:</i></p>

### Claim 1

### Accused Products

Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138\_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6

Claim 1	Accused Products
	 <p>The circuit diagram illustrates a current sink for a NAND flash. It includes several input signals: GVBN, VHACKS_EN, VHA_LDDET2, VHA_LDDET1, VHA_CTL1[1], VHA_CTL1[0], VHA_CTL1[2], VHA_LDDET4, and VHA_SWEN. The circuit is composed of multiple PMOS and NMOS transistors with specified W/L ratios. A blue callout box points to a PMOS transistor with the text "a load selector means".</p>
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

Claim 1	Accused Products
	 <p>output of the pumping circuit</p> <p>associated with a specific pump voltage</p> <p>selectively coupling a load</p> <p>a load selector means</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

**Claim 2**

Claim 2	Accused Products
2. The charge pump circuit of claim 1, wherein the load	To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means includes a target output pump selector for shutting down

Claim 2	Accused Products
<p>selector means includes a target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or equal to a reference voltage (Vref).</p>	<p>the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or equal to a reference voltage (Vref).</p> <p>For example, in the Dell/EMC XPS 15 2-in-1 9575, VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72) adjusts the output reference voltage by shorting out resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping.</p> <p><i>See evidence and explanation for claim element [1a], supra.</i></p>

**Claim 3**

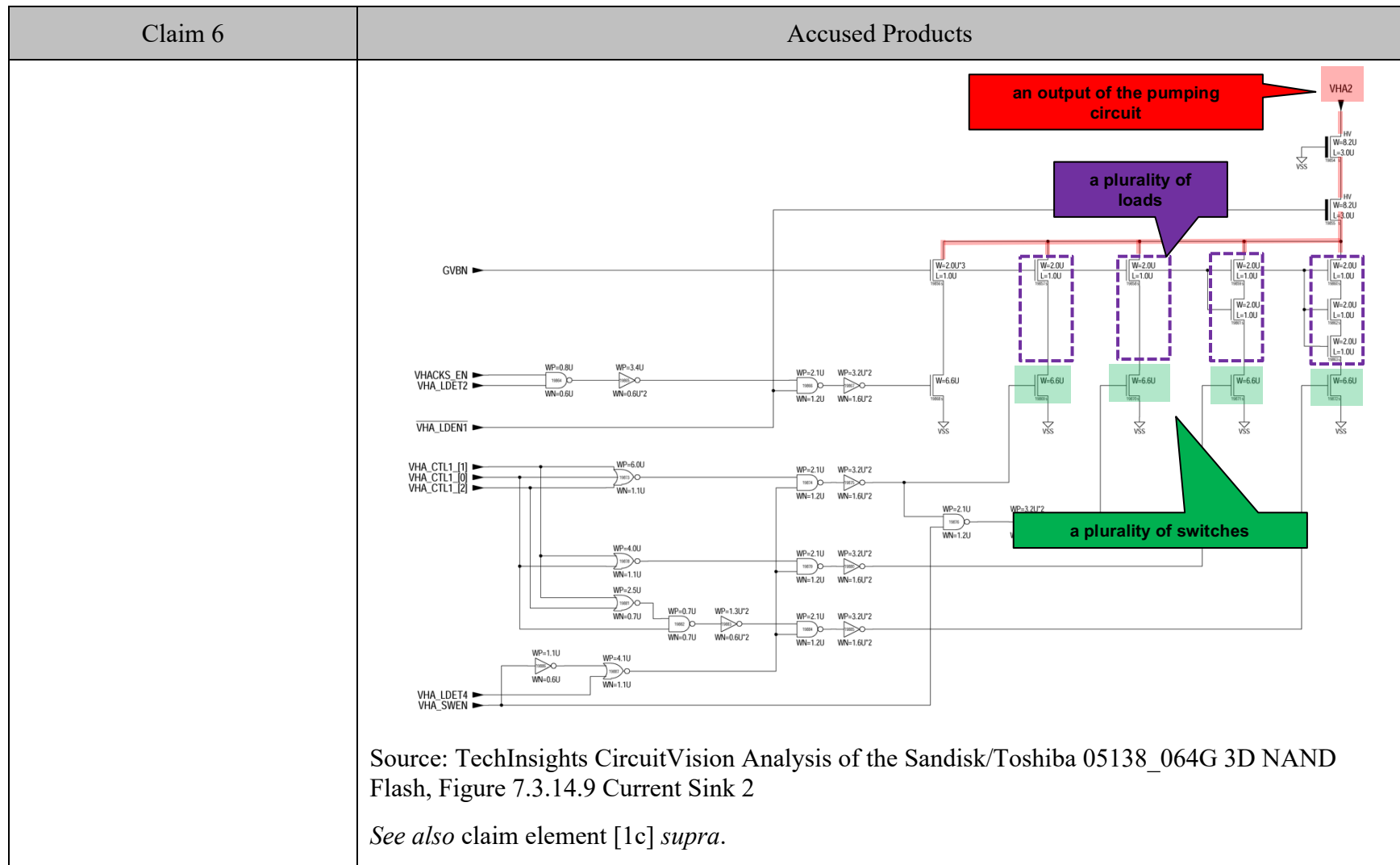
Claim 3	Accused Products
<p>3. The charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, and whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is less than or equal to the reference voltage (Vref).</p> <p><i>See evidence and explanation for claim element [1a] and claim 2, supra.</i></p>



Claim 3	Accused Products
less than or equal to the reference voltage ( $V_{ref}$ ).	

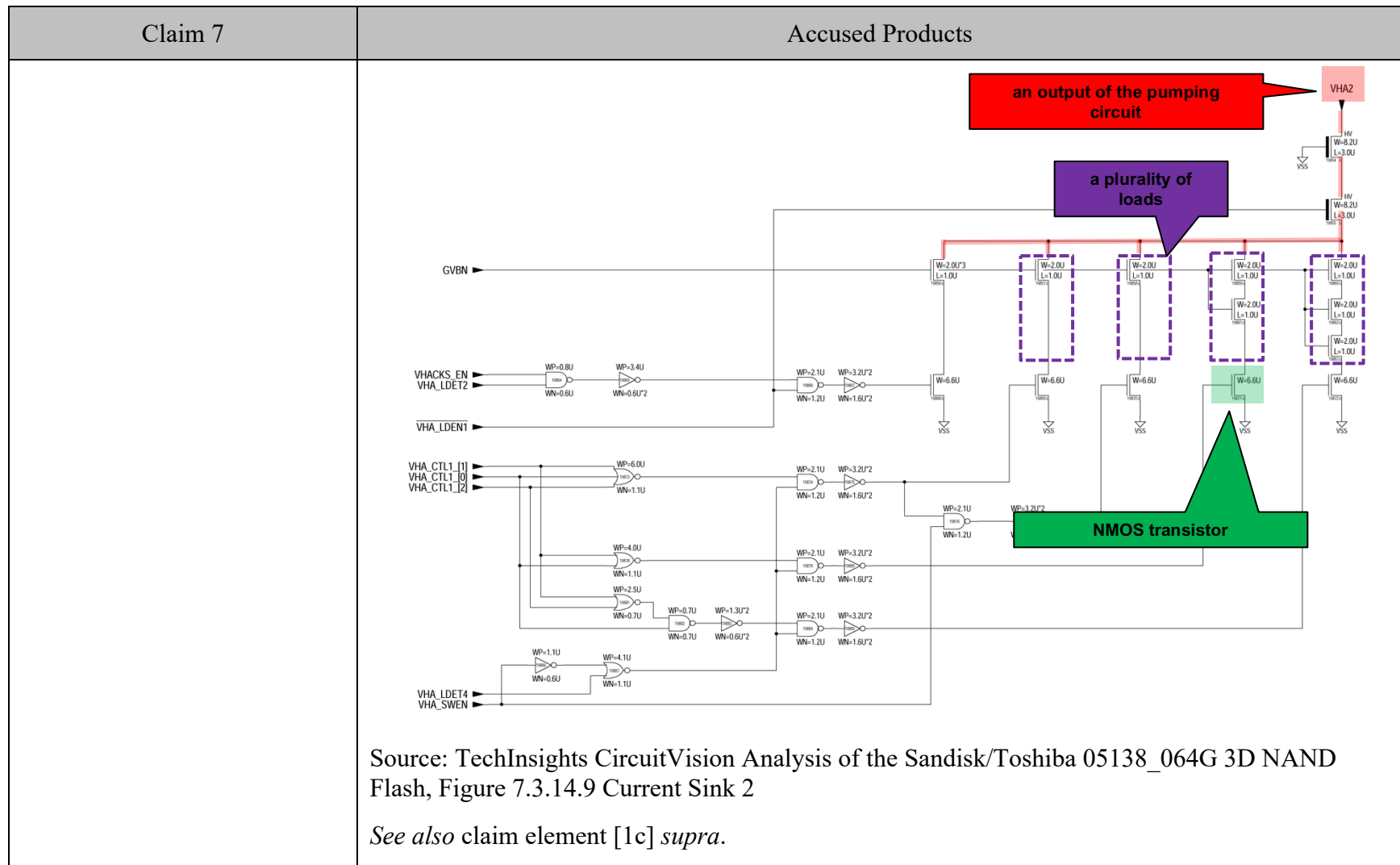
**Claim 6**

Claim 6	Accused Products
6. The charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.</p> <p><i>See, e.g.:</i></p>



**Claim 7**

Claim 7	Accused Products
<p>7. The charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p> <p><i>See, e.g.:</i></p>



**Claim 8**

Claim 8	Accused Products
<p>8. The charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p> <p><i>See, e.g.:</i></p>

<p>Claim 8</p>	<p>Accused Products</p>
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p> <p>See also claim element [1c] <i>supra</i>.</p>

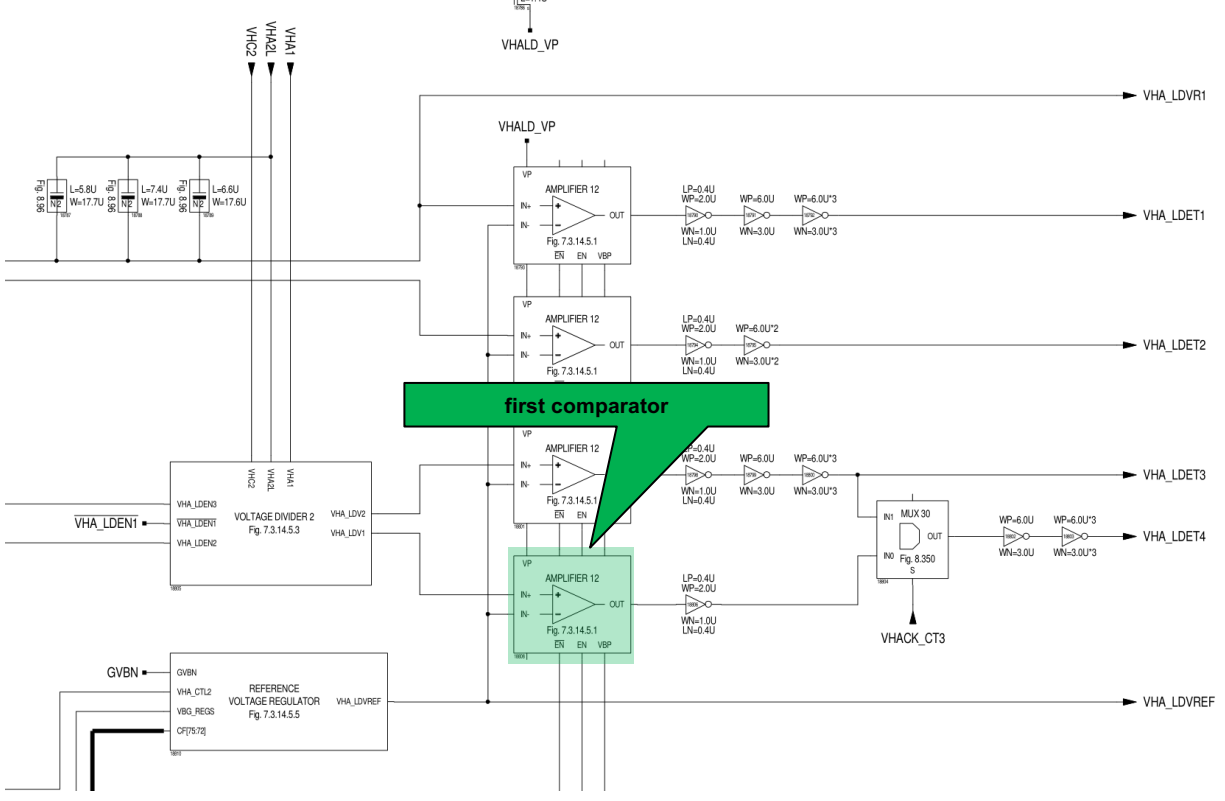
**Claim 11**

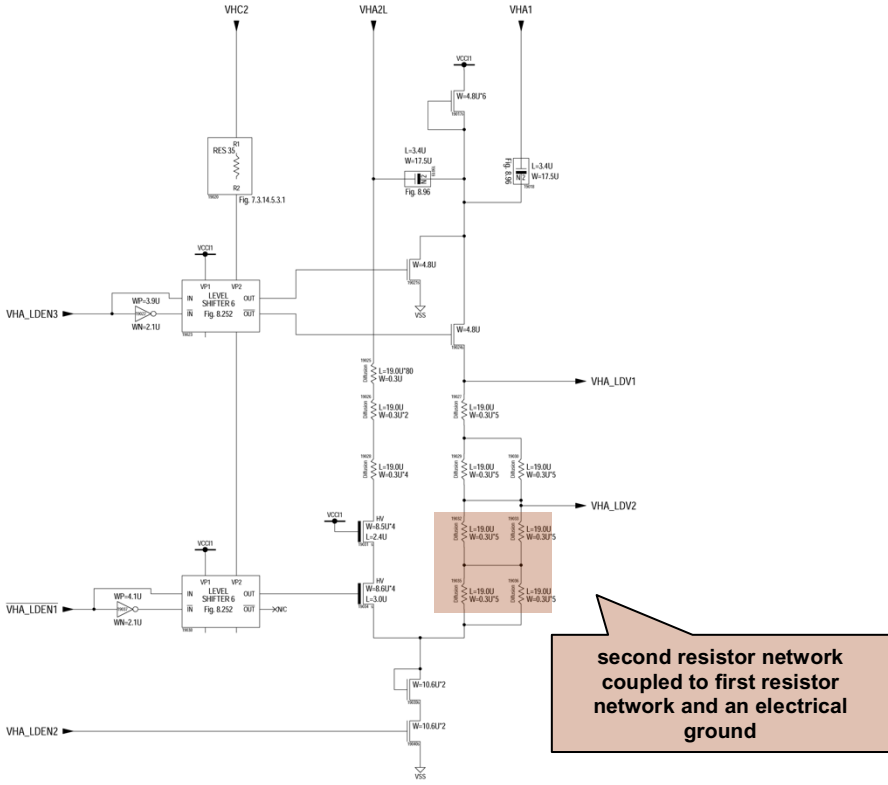
Claim 11	Accused Products
[11pre] 11. The charge pump circuit of claim 2 wherein the target output pump selector comprises:	Each Accused Product includes the charge pump circuit of claim 2. <i>See supra</i> claim 2.
[11a] a) a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref);	Each Accused Product includes a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref). <i>See, e.g.:</i>

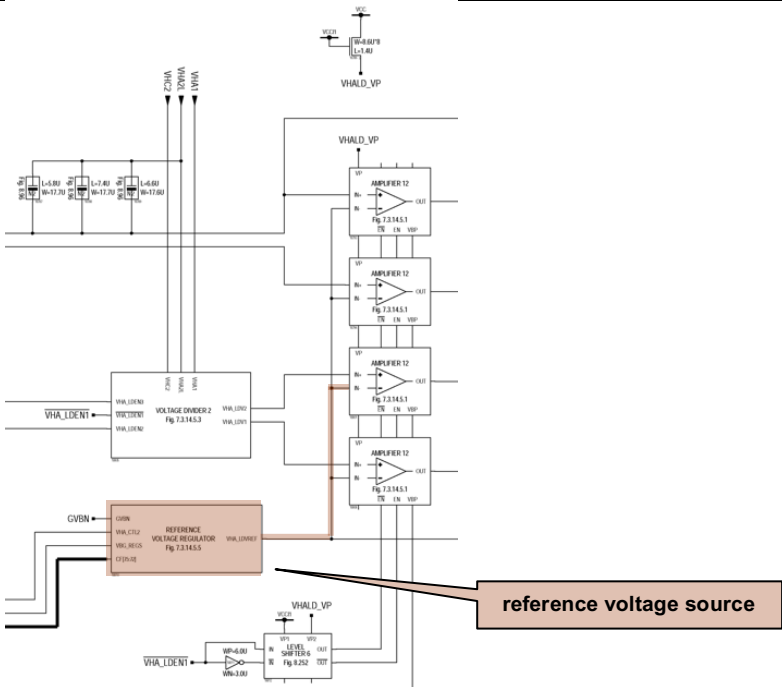
Claim 11	Accused Products
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>
<p>[11b] b) a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator;</p>	<p>Each Accused Product includes a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator.</p> <p><i>See, e.g.:</i></p>



Claim 11	Accused Products
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2; Figure 7.3.14.5 Level Detector 6</p>

Claim 11	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>
<p>[11c] c) a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the</p>	<p>Each Accused Product includes a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being coupled to an electrical ground.</p> <p><i>See, e.g.:</i></p>

Claim 11	Accused Products
<p>second resistor network being coupled to an electrical ground; and</p>	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2</p>
<p>[11d] d) a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.</p>	<p>Each Accused Product includes a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.</p> <p>See, e.g.:</p>

Claim 11	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>